CLAIMS

What is claimed is:

1. A computer system comprising:

a memory; and

a memory controller, wherein the memory controller includes a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

2. The computer system of claim 1, wherein the refresh timing circuit triggers memory refresh events whenever the computer system is operating in a normal mode and a low power mode.

3. The computer system of claim 2, wherein the refresh timing circuit further comprises:

a clock generator for generating the clock pulses;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

4. The computer system of claim 3, wherein the first counter counts the number of clock pulses generated by the clock generator.

5. The computer system of claim 4, wherein the first counter transmits data to the storage register whenever the computer system is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a prior memory refresh event.

6. The computer system of claim 5, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

7. The computer system of claim 6, wherein the first counter transmits signals to the comparator whenever the computer system is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

8. The computer system of claim 7, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

9. The computer system of claim 4, wherein the refresh timing circuit further comprises a second counter.

10. The computer system of claim 9, wherein the first counter counts the number of clock pulses generated by the clock generator while the computer system is operating in the low power mode and the second counter counts the number of clock pulses generated by the clock generator while the computer system is operating in a normal mode.

11. The computer system of claim 10, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the computer system is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

12. The computer system of claim 11, wherein the second counter is deactivated and the first counter is activated whenever the computer system transitions from the normal mode to the low power mode.

13. The computer system of claim 12, wherein the first counter transmits signals to the comparator whenever the computer system is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

14. The computer system of claim 3, wherein the refresh timing circuit includes a second counter for triggering memory refresh events whenever the computer system is operating in the normal mode

15. The computer system of claim 1, wherein the memory is an Extended Data Out Dynamic Random Access Memory (EDO DRAM) and the memory controller is an EDO DRAM controller.

16. An Extended Data Out Dynamic Random Access Memory (EDO DRAM) controller comprising:

a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

17. The computer system of claim 16, wherein the refresh timing circuit further comprises:

a clock generator;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

18. The EDO DRAM controller of claim 17, wherein the EDO DRAM controller operates in a normal mode and a low power mode.

19. The EDO DRAM controller of claim 18, wherein the first counter counts the number of clock pulses generated by the clock generator.

20. The EDO DRAM controller of claim 19, wherein the first counter transmits data to the storage register whenever the EDO DRAM controller is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

21. The EDO DRAM controller of claim 20, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

22. The EDO DRAM controller of claim 21, wherein the first counter transmits signals to the comparator whenever the EDO DRAM controller is operating in the

low power mode, the signal representing the number of clock pulses received from the clock generator.

23. The EDO DRAM controller of claim 22, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

24. The EDO DRAM controller of claim 19, wherein the refresh timing circuit further comprises a second counter.

25 . The EDO DRAM controller of claim 24, wherein the first counter counts the number of clock pulses generated by the clock generator while the EDO DRAM controller is operating in the low power mode and the second counter counts the number of clock pulses generated by the clock generator while the EDO DRAM controller is operating in the normal mode.

26. The EDO DRAM controller of claim 25, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the EDO DRAM controller is operating in the normal mode, the data representing the

number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

27. The EDO DRAM controller of claim 26, wherein the second counter is deactivated and the first counter is activated whenever the EDO DRAM controller transitions from the normal mode to the low power mode.

28. The EDO DRAM controller of claim 27, wherein the first counter transmits signals to the comparator whenever the EDO DRAM controller is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

29. A method of calibrating a refresh timer in a computer system, the method comprising:

counting a first set of clock pulses received at a counter from a clock generator;

receiving a signal indicating that a memory refresh event has been triggered; and

storing a first count representing the number of clock cycles received at the counter before receiving the signal.

30. The method of claim 29, further comprising:

resetting the counter after storing the first count;

counting a second set of clock pulses;

receiving the signal indicating that a memory refresh event has been triggered; and

storing a second count.

31. The method of claim 29, wherein the refresh timer is a low power mode refresh timer.

32. In a computer system having a normal mode of operation and a low power mode of operation, a method of triggering a memory refresh event while the computer system is operating in the low power mode, the method comprising:

transmitting a frequency value to a comparator, the frequency value representing the frequency at which to trigger memory refresh events;

transmitting a first clock pulse count to the comparator;

determining whether the first clock pulse count is equal to the frequency value; and

transmitting a first refresh signal.

33. The method of claim 32, further comprising:

transmitting a second clock pulse count to the comparator if it is determined that the first clock pulse is not equal to the frequency value;

determining whether the second clock pulse count is equal to the frequency value; and

transmitting the first refresh signal.

34. The method of claim 32, further comprising transitioning from the normal mode of operation to the low power mode of operation before transmitting the frequency value to the comparator.

35. The method of claim 32, wherein the process of transmitting the first clock pulse count to the comparator further comprises:

transmitting a clock pulse from a clock generator to a counter;

incrementing the counter; and

transmitting the incremented count to the comparator.

36. The method of claim 35, further comprising resetting the counter before transmitting the clock pulse from the clock generator.

37. The method of claim 35, further comprising:

resetting the counter after transmitting the refresh signal;

transmitting a second clock pulse count to the comparator;

determining whether the second clock pulse count is equal to the frequency value; and

transmitting a second refresh signal.